



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

H.A.

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/510,679	10/08/2004	Yoshinori Miyaki	XA-10186	4946

181 7590 12/28/2006  
MILES & STOCKBRIDGE PC  
1751 PINNACLE DRIVE  
SUITE 500  
MCLEAN, VA 22102-3833

EXAMINER
----------

KUNZER, BRIAN

ART UNIT	PAPER NUMBER
----------	--------------

2814

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/28/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

10/510,679

Applicant(s)

MIYAKI ET AL.

Examiner

Brian Kunzer

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 21 November 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 58-87 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 58-87 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 21<sup>st</sup>, 2006 has been entered.

### *Amendments*

The amendment filed November 21<sup>st</sup>, 2006 has been received and entered. In summary, claim 58 has been amended and new claims 68-87 have been added.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 58-60, 62-66, 68-70, 72-76, 78-80, and 82-86 are rejected under 35 U.S.C. 103(a) unpatentable over Li (USPN. 6,348,729) in view of Jung (USPN. 6,342,730).

With respect to claim 58, Li teaches, from figs. 6-10 and columns 3 and 4, a method of manufacturing a semiconductor device, comprising the steps of:

(a) providing a tape (250) having a main surface, a back surface opposed to the main surface, a product forming portion formed on the main surface, and a plurality of terminals (222a, 224) formed in a product forming portion (see column 3, lines 16-26); (fig. 6)

(b) fixing a semiconductor element (210) to the main surface of the tape (250); (fig. 7)

(c) electrically connecting a plurality of electrodes (212) formed over the semiconductor element (210) with the plurality of terminals (222a, 224) through wires (230, 232); (fig. 8)

(d) sealing the semiconductor element (210), the wires (230, 232), the plurality of terminals (222a, 224), and the main surface of the tape (250) with a resin (240), and forming a sealing member; (fig. 9)

(e) after the step (d), peeling the tape (250) from the sealing member, and thereby exposing a part of each of the plurality of terminals (222a, 224) from the sealing member; (fig. 10) and

(f) forming a metal layer (solder paste) over the part of each of the plurality of terminals (222a, 224),

wherein the metal layer is formed by a printing process. (See the described process of forming leads attached to the terminals (leads) (222a, 224) in column 4, line 61- column 5, line 5.)

Li does not specifically teach the semiconductor device wherein there is no exposure of the plurality of terminals and terminal leads at outer edges of the sealing member. [Also in regards to this limitation it has been held that to be entitled to weight in method claims, the recited-structure limitations therein must affect the method in a manipulative sense, and not to

Art Unit: 2814

amount to the mere claiming of a use of a particular structure. Ex parte Pfeiffer, 1962 C.D. 408 (1961).]

However, Jung, drawn to encapsulated wire bonded chip packages, teaches from fig. 2, a semiconductor device wherein there is no exposure of the plurality of terminals (250) and terminal leads (230) at outer edges of the sealing member (220).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device of Li feature wire bond terminals that are only exposed on their bottom electrical contact surfaces as disclosed by Jung, since this provides enhanced enclosure and protection of the terminals while increasing adhesion of the terminals with the sealing member. (See column 3, lines 1-7, and column 4, lines 44-65.)

With respect to claim 68, Li teaches, from figs. 6-10 and columns 3 and 4, a method of manufacturing a semiconductor device, comprising the steps of:

(a) providing a tape (250) having a main surface, a back surface opposed to the main surface, a product forming portion formed on the main surface, and a plurality of terminals (222a, 224) formed in a product forming portion (see column 3, lines 16-26); (fig. 6)

(b) fixing a semiconductor element (210) to the main surface of the tape (250); (fig. 7)

(c) electrically connecting a plurality of electrodes (212) formed over the semiconductor element (210) with the plurality of terminals (222a, 224) through wires (230, 232); (fig. 8)

(d) sealing the semiconductor element (210), the wires (230, 232), the plurality of terminals (222a, 224), and the main surface of the tape (250) with a resin (240), and forming a sealing member; (fig. 9)

Art Unit: 2814

(e) after the step (d), peeling the tape (250) from the sealing member, and thereby exposing a part of each of the plurality of terminals (222a, 224) from the sealing member; (fig. 10) and

(f) forming a metal layer (solder paste) over the part of each of the plurality of terminals (222a, 224),

wherein the metal layer is formed by a printing process. (See the described process of forming leads attached to the terminals (leads) (222a, 224) in column 4, line 61- column 5, line 5.)

Li does not specifically teach the semiconductor device wherein there is no exposure of the plurality of terminals and terminal leads at side edges of the sealing member. [Also in regards to this limitation it has been held that to be entitled to weight in method claims, the recited-structure limitations therein must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure. Ex parte Pfeiffer, 1962 C.D. 408 (1961).]

However, Jung, drawn to encapsulated wire bonded chip packages, teaches from fig. 2, a semiconductor device wherein there is no exposure of the plurality of terminals (250) and terminal leads (230) at side edges of the sealing member (220).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device of Li feature wire bond terminals that are only exposed on their bottom electrical contact surfaces as disclosed by Jung, since this provides enhanced enclosure and protection of the terminals while increasing adhesion of the terminals with the sealing member. (See column 3, lines 1-7, and column 4, lines 44-65.)

With respect to claim 78, Li teaches, from figs. 6-10 and columns 3 and 4, a method of manufacturing a semiconductor device, comprising the steps of:

(a) providing a tape (250) having a main surface, a back surface opposed to the main surface, a product forming portion formed on the main surface, and a plurality of terminals (222a, 224) formed in a product forming portion (see column 3, lines 16-26); (fig. 6)

(b) fixing a semiconductor element (210) to the main surface of the tape (250); (fig. 7)

(c) electrically connecting a plurality of electrodes (212) formed over the semiconductor element (210) with the plurality of terminals (222a, 224) through wires (230, 232); (fig. 8)

(d) sealing the semiconductor element (210), the wires (230, 232), the plurality of terminals (222a, 224), and the main surface of the tape (250) with a resin (240), and forming a sealing member; (fig. 9)

(e) after the step (d), peeling the tape (250) from the sealing member, and thereby exposing a part of each of the plurality of terminals (222a, 224) from the sealing member; (fig. 10) and

(f) forming a metal layer (solder paste) over the part of each of the plurality of terminals (222a, 224),

wherein the metal layer is formed by a printing process. (See the described process of forming leads attached to the terminals (leads) (222a, 224) in column 4, line 61- column 5, line 5.)

Li does not specifically teach the semiconductor device wherein the plurality of terminals and terminal leads are exposed from only a bottom surface of the sealing member. [Also in regards to this limitation it has been held that to be entitled to weight in method claims, the

Art Unit: 2814

recited-structure limitations therein must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure. Ex parte Pfeiffer, 1962 C.D. 408 (1961).]

However, Jung, drawn to encapsulated wire bonded chip packages, teaches from fig. 2, a semiconductor device wherein the plurality of terminals (250) and terminal leads (230) are exposed from only a bottom surface of the sealing member (220).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the device of Li feature wire bond terminals that are only exposed on their bottom electrical contact surfaces as disclosed by Jung, since this provides enhanced enclosure and protection of the terminals while increasing adhesion of the terminals with the sealing member. (See column 3, lines 1-7, and column 4, lines 44-65.)

With respect to claims 59, 69, and 79, all claims comprising similar subject matter, Li teaches, from figs. 6-10 and columns 3, lines 34-63, the method wherein the plurality of terminals (222a, 224) are formed by affixing a metal foil (copper foil) to the main surface of the tape and thereafter etching the metal foil selectively.

With respect to claim 60, 70, and 80, all claims comprising similar subject matter, Li teaches, from figs. 6-10 and columns 3, lines 34-63, the method wherein the metal foil (copper) is affixed to the main surface of the tape through a first adhesive (polyimide).

With respect to claim 62, 72, and 82, all claims comprising similar subject matter, Li teaches, from fig. 10, the method wherein a back surface of the semiconductor element (210) is exposed from the sealing member.

With respect to claim 63, 73, and 83, all claims comprising similar subject matter, Jung teaches from figs. 2 and 9, a tape (260) has a semiconductor element fixing piece (232), and the semiconductor element (210) is mounted over the semiconductor element fixing piece (232).

With respect to claim 64, 74, and 84, all claims comprising similar subject matter, Li teaches, from figs. 6-10 and columns 3, lines 34-67, the method wherein the plurality of terminals (222a, 24) are fixed to the tape (250) through a first adhesive (the polyimide in the tape), and the semiconductor element (210) is fixed to the tape through a second adhesive (not shown, thermosetting adhesive, column 3, lines 65-67).

With respect to claim 65, 75, and 85, all claims comprising similar subject matter, Examiner takes the position that the material selected for the adhesive layer under the semiconductor element, in view of those used in the prior art, is non-critical to the applicant's invention. Li discloses all the limitations of the claimed invention - including gold or silver plating on the leads (222a, 224) (see column 3, lines 10-35) - except for specifically teaching that "a Pd plating film is formed over each of the plurality of terminals." It would have been obvious to one of ordinary skill in the art, at the time of invention, to have the gold or silver plating of Li's device to utilize palladium (Pd) instead, since it has been held to be within the general skill

Art Unit: 2814

of a person in the art to select a known material on the basis of its suitability for the intended use (to provide better bonding for conductive wires from the semiconductor element) as a matter of obvious design choice. *In re Leshin*, 227 F.2d 197, 125 USPQ 416 (CCPA 1960). Also, column 3, lines 7-25 of Jung et al. (USPN 6,342,730) is provided as further support of this position.

With respect to claim 66, 76, and 86, all claims comprising similar subject matter, Li teaches, from figs. 6-10 and columns 3, lines 34-67, the method wherein the tape is formed by a resin film selected from polyimide resin, ethylene-vinylacetate copolymer resin, polyolefin resin and methacrylate resin.

2. Claims 61, 71, and 81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US Patent No. 6,348,729) and Jung (USPN. 6,342,730) as applied to claims 59, 69, and 79 above, and further in view of Narushima (US Patent No. 5,298,304).

Li teaches, from figs. 6-10 and columns 3, lines 34-63, the method wherein the metal foil is bonded to the tape.

Li does not state that the metal foil is specifically compression-bonded to the tape by thermocompression bonding. This is most likely inherent though, as this is a well-known and commonly used method of forming TAB tape.

Nevertheless, Narushima, drawn to adhesive tapes for tape automated bonding (TAB), teaches from column 1, lines 15-51, that metal (copper) foil compression-bonded to the (adhesive) tape by thermocompression bonding is known.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the tape as described by Li be specifically formed by thermocompression bonding as disclosed by Narushima, since this forms a laminated tape suitable for TAB processes. (See column 1, lines 15-51.)

3. Claims 67, 77, and 87 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US Patent No. 6,348,729) and Jung (USPN. 6,342,730) as applied to claims 58, 68, and 78 above, and further in view of Long (US Patent No. 5,173,766).

Li teaches, from figs. 6-10, the method as stated above.

Li does not teach that step (d) is carried out while the back surface of the tape is held by vacuum suction.

However, Long, drawn to the manufacture of semiconductor packages, teaches, from figs. 6A and 6B, vacuum suction (through 610,a,b) is used to hold the back surface of the tape (551) in the step of fixing a semiconductor element (24) to a carrier tape assembly (551). Also, vacuum suction (through hole 710b) used during wire connection process. (See fig. 7a and column 26, lines 34-37.)

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the method of chip manufacturing of Li utilizing a vacuum suction process - as described by Long - to hold the tape in place during chip placement, wiring connection, or resin molding steps because this process provides a stable and accurate environment for these steps to be carried out (see column 26, lines 44-46) and the fact that vacuum holding is well known in the art. (See column 3, lines 28-32)

***Response to Arguments***

4. Applicant's arguments with respect to claims 58-87 have been considered but are moot in view of the new ground(s) of rejection.

Applicant makes the following argument in regards to the newly submitted claims

58-67:

For example, Li teaches that the lower surface of the lead frame and the backside surface of the die are exposed through the plastic body. See Li, Abstract; col. 3, lines 27-34; Fig. 12. In particular, Li clearly shows in Fig. 12 that his leads (222) are exposed at outer edges of the plastic package body (240). Therefore, Li does not teach or suggest a method of manufacturing wherein there is no exposure of the plurality of terminals and terminal leads at outer edges of the sealing member as recited in Claim 58.

None of the secondary references remedy this deficiency of Li. Therefore, Applicants' respectfully submit that Claim 58 patentably distinguishes over the applied prior art.

Applicant is referred to figs. 1, 2, 10, and 11 of Jung et al. (USPN. 6,342,730) which does teach these features.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Kunzer whose telephone number is (571) 272-5054. The examiner can normally be reached on Monday-Friday 8:00-4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2814

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK  
12/20/06



ANH D. MAI  
PRIMARY EXAMINER